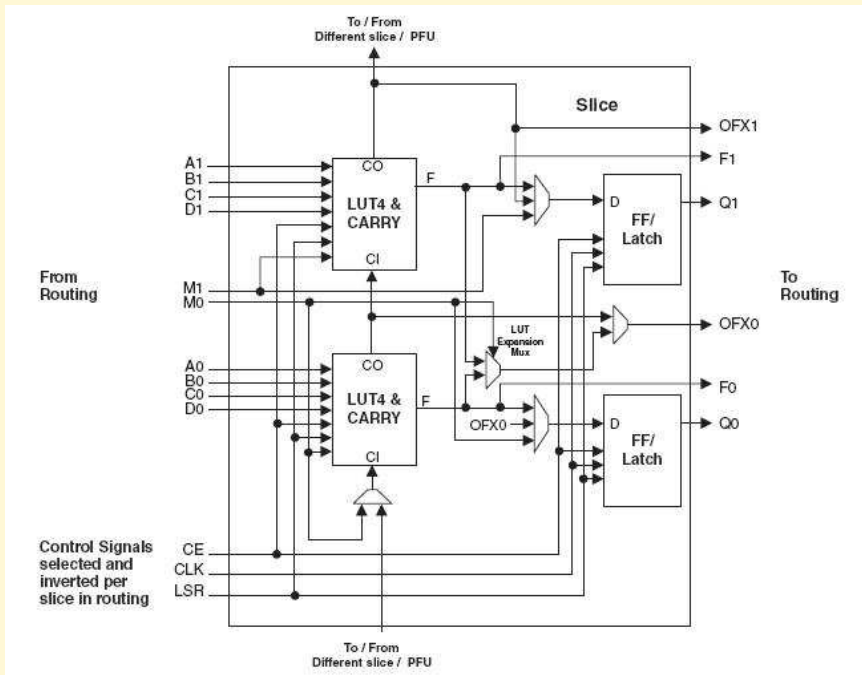


Linux and FPGAs

Chad D. Kersey
chad@cdkersey.com



- Reconfigurable logic and interconnect.
- Divided into *slices* as pictured above.
- Each slice combinational or sequential.
- RAM, IO, and other IP typically included.

- Start hardware production before design complete. (Like, for instance, the Open Graphics Project)
- Produce small-run or one-time custom designs cheaply.
- Simulate hardware before it's produced.
- Accelerate highly parallel applications (like genome sequencing)

[FPGA Overview](#)

[Architecture](#)

[Applications](#)

[FPGA Development in Linux](#)

[Linux on FPGA Devices](#)

HDL-Based Development

- Basis of hardware design on FPGAs.
- Enhanced by IP libraries, floorplanning tools.
- Free cores available to include in your designs.

```
mem[4] = 12'o0000; mem[10] = 12'o0000; mem[16] = 12'o0000;
mem[5] = 12'o0000; mem[11] = 12'o0000; mem[17] = 12'o0000;
end

/*Set up the clock pulse*/
always
begin
#10 clk = ~clk;
end

always @(posedge clk) begin
/*Fetch*/
ir = mem[pc];

/*Decode/Execute*/
if ( ir[11:9] == 0 ) begin
/*Add*/
regs[ir[8:6]] = regs[ir[5:3]] + regs[ir[2:0]];
end else if ( ir[11:9] == 1 ) begin
/*And*/
regs[ir[8:6]] = ~(regs[ir[5:3]] & regs[ir[2:0]]);
end else if ( ir[11:9] == 2 ) begin
/*Load*/
regs[ir[8:6]] = mem[regs[ir[5:3]] + ir[2:0]];
end else if ( ir[11:9] == 3 ) begin
/*Store*/
mem[regs[ir[5:3]] + ir[2:0]] = regs[ir[8:6]];
end else if ( ir[11:9] == 4 ) begin
/*Shift*/

architecture VgaController_a of VgaController is
type linestyle_t is (
frontporch, hsync, backporch, lborder, video, rborder
);
type fieldstate_t is (
frontporch, vsync, backporch, tborder, video, bborder, reset
);
signal linestyle ; linestyle_t;
signal fieldstate ; fieldstate_t;
signal linebuffer ; std_logic_vector(159 downto 0);
signal counter ; std_logic_vector(7 downto 0);
begin
with linestyle select
hsync_out <= '0' when hsync,
'1' when others;
with fieldstate select
vsync_out <= '0' when vsync,
'1' when others;
process (clock, resetn)
begin
if resetn = '0' then fieldstate <= reset;
elsif (rising_edge(clock)) then
case fieldstate is
```

FPGA Overview

FPGA Development in Linux

HDL-Based Development

Free Cores

Free Simulation Tools

Commercial Tools

Linux on FPGA Devices

- Open Cores (opencores.org) has many useful projects, including free processors, network devices, and video interfaces.
- The Open Graphics Project (wiki.opengraphics.org) aim to produce a free hardware GPU.
- LEON (www.gaister.com/leonmain.html) is an open-source SPARC core written in VHDL that is synthesizable on an FPGA.

[FPGA Overview](#)

[FPGA Development in Linux](#)

[HDL-Based Development](#)

[Free Cores](#)

[Free Simulation Tools](#)

[Commercial Tools](#)

[Linux on FPGA Devices](#)

Free Simulation Tools

- Icarus Verilog (www.icarus.com/eda/verilog) is an open source simulator supporting a useful subset of the Verilog HDL.
- GHDL (ghdl.free.fr) is a GHDL simulation environment built around GCC.
- GTK-Wave (home.ne.rr.com/gtkwave) is a waveform viewer compatible with GHDL and iverilog.
- These can be combined with an appropriate text editor and build system to create a productive custom hardware design environment.

[FPGA Overview](#)

[FPGA Development in Linux](#)

[HDL-Based Development](#)

[Free Cores](#)

[Free Simulation Tools](#)

[Commercial Tools](#)

[Linux on FPGA Devices](#)

Free-of-Charge Educational Licensing

- Xilinx ISE (www.xilinx.com/ise)
- ModelSim (www.model.com) More complete language support than GHDL or iverilog, with integrated waveform editor and viewer, carries steep fees for commercial use.

For-pay Only

- Altera Quartus II (www.altera.com), an HDL-based integrated development environment for Altera FPGA's.

[FPGA Overview](#)

[FPGA Development in Linux](#)

[HDL-Based Development](#)

[Free Cores](#)

[Free Simulation Tools](#)

[Commercial Tools](#)

[Linux on FPGA Devices](#)

μ CLinux on Soft Cores

- uCLinux gives Linux-like driver support and environment without requiring hardware memory protection (expensive to implement).
- Altera NIOS (www.niosforum.com) runs a variant of uCLinux natively.
- The LEON SPARC Implementation (www.gaisler.com/leonmain.html) runs uCLinux.

FPGA Overview

FPGA Development in Linux

Linux on FPGA Devices

μ CLinux on Soft Cores

Embedded Processor Cores

Embedded Processor Cores



- Xilinx Platform Studio (part of ISE) supports MontaVista Linux as a default target environment.
- Used in SBC design evaluation, prototyping, and systems research.

FPGA Overview

FPGA Development in Linux

Linux on FPGA Devices

μ CLinux on Soft Cores

Embedded Processor Cores